Amendments to the Specification:

Please replace the paragraph beginning at page 5, line 15, with the following rewritten paragraph:

-- The requirement of higher clock rates has lead to the use of copper to form the metal interconnect lines in integrated circuits. In addition to the use of copper, dielectric layers such as organosilicate glass (OSG) (dielectric constant ~2.6) and florosilicate glass (FSG) are currently being used to take advantage of the lower dielectric constant of such materials compared to silicon dioxide. In an embodiment of the instant invention, a first etch stop layer 130 is formed over a copper layer 120 and a dielectric layer 100 as shown in Figure 2(a). The dielectric layer 100 is formed over a silicon substrate which contains one or more electronic devices such as transistors, diodes, etc. These electronic devices will typically be part on of an integrated circuit. The dielectric layer 100 may be formed over various portions of an integrated circuit. The copper layer 120 represents a portion of the copper interconnect of the integrated circuit. The first etch stop layer 130 may comprise silicon nitride (SiN), silicon carbide (SiC), or any suitable material. Following formation of the first etch stop layer 130, a first dielectric film 140 is formed over the etch stop layer 130. In an embodiment of the instant invention this first dielectric layer 140 comprises florosilicate glass (FSG) which has a dielectric constant of about. In addition to FSG any suitable dielectric material may be used to form the first dielectric layer 140. Following the formation of the first dielectric layer 140, a second etch stop layer 150 may or may not be formed. This second etch stop layer 150 comprises a material selected from the group consisting of silicon nitride (SiN), silicon carbide (SiC), or any combination of layers of these or other

suitable materials. Following the formation of the second etch stop layer 150, a second dielectric layer is formed. In an embodiment of the instant invention this second etch stop layer comprises FSG, OSG or any suitable dielectric material. Following the formation of the second dielectric layer 160, a layer of anti-reflective coating (ARC) 170 is formed as shown in Figure 2(a). In an embodiment of the instant invention this ARC layer 170 comprises silicon oxynitride. An important property of the ARC layer 170 is that no light be reflected during the photolithographic process. Such an ARC film can be formed using silicon oxynitride with the following atomic percentages, silicon (30% -55%), oxygen (20% - 50%), nitrogen (2% - 17%), and hydrogen (7% - 35%). Following the formation of the ARC layer 170, a photoresist layer is formed and patterned 180. The ARC layer 170, the second dielectric layer 160 and the second etch stop layer 150 are etched using a multi-step etch process to form a first trench 185 as illustrated in Figure 2(a). In an embodiment of the instant invention the silicon oxynitride layer can be etched using a CF₄ based plasma etch process. In particular a 300A to 2000A silicon oxynitride film can be etched using CF₄ with flow rates of 50sccm – 120sccm, oxygen with flow rates of 1sccm – 9sccm, argon with flow rates of 200sccm – 500sccm, and power of about 1000W to 2000W. One advantage of using the silicon oxynitride film is that thinner layers of photoresist (i.e. less than 3000A) can be used. This leads to improved resolution over the thicker resist films necessary in current processes. For cases where FSG is used to form the second dielectric layer 160, an argon (200sccm -400sccm), CH₂F₂ (10sccm – 35sccm), and oxygen (9sccm – 34sccm) based plasma etch process can be used with power levels of approximately 1000W. Finally to etch through the second etch stop layer 150, a C₅F₈ (5sccm – 13sccm), argon (300sccm –

650sccm), and oxygen (4sccm – 13sccm) etch process with a power level of approximately 1500W can be used. The depth of the first trench 187 is variable. The embodiment represented in Figure 2(a) shows the bottom surface of the trench below the second etch stop layer. In general the required depth of the first trench depends on the thickness of the dielectric layers 140 and 160 and the required depth of the second trench.--